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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,095	07/29/2003	Wolfgang Ramin	TID-32348	6377

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,095	RAMIN, WOLFGANG	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-15 drawn to a semiconductor device is acknowledged.

Claim Objections

2. Claim 8 is objected to because of the following informalities: The unit for the chip thickness as recited in claim 8, 2nd line appears to have a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Okamoto et al., US patent No. 6,630,734.

Regarding claim 1, Okamoto teaches (fig. 18) an encapsulated chip assembly comprising (col. 15, lines 47-57): a baseplate (70), a chip (65, IC) attached to the baseplate in such a way that its contact surfaces (the top surface of 65) face away from the baseplate (70), a layer (69) of a conductive material applied to the baseplate (12) and arranged to around the chip (65 refer to figure 18), and which is at least as high as the chip (65), a cover plate (73) arranged on the layer of conductive material (69),

whose one side, opposing the chip (65), being provided with one or more conductive surfaces (72), which are arranged in such a way that they form an electrical connection between the chip (65) and the layer of conductive material (69).

Regarding claim 6, Okamoto teaches the entire claimed structure of claim 1, above including both the baseplate (70) and the cover plate (73) each consist of a flexible material. The base is formed of a composite material that is nickel-plated and the cover plate (73) is formed of a resin material that are both flexible.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto in view of Nakaoka et al. US patent No. 6,583,512.

Regarding claim 2, Okamoto teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the chip is surrounded by a filler material that fills the open space between the baseplate and the cover plate.

Nakaoka teaches the use of a filler material (30, col. 11, lines 64-67) in order to fill the space between the semiconductor devices (fig. 8c).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the filler material taught by Nakaoka in the structure of Okamoto in order to seal the device.

Regarding claim 3, Okamoto teaches substantially the entire claimed structure of claims 1 and 2 above including further comprising an electrically conductive glue (72, TAB), which is to establish both the electrical and the mechanical connections between the contact surfaces (top surface of 65) of the chip (65) and of the cover plate (73).

Regarding claim 4, Okamoto teaches substantially the entire claimed structure of claims 1 and 2 above including further comprising an anisotropically conductive film (30, col. 11, lines 64-67) (ACF), which serves to establish both an electrical and a mechanical connection between the contact surfaces (top surface of 65) of the chip (65) and the conductive surface (72) or the conductive surfaces, respectively, of the cover plate (73).

Regarding claim 5, Okamoto teaches substantially the entire claimed structure of claims 1 and 2 above including the filler material consists of the anisotropically conductive film (col. 11, lines 64-67).

7. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto.

Regarding claims 7-8, Okamoto teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the height of the chip is so low that it is rendered flexible or has a thickness of less than 50 micrometer. Since most integrated circuits use silicon Okamoto teaches a chip that consists mainly of silicon.

Parameters such as height in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the height of the IC of Okamoto as claimed in order to form a device that is easily packaged.

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto, in view of Loeffler et al. US patent No. 5,838,074.

Regarding claim 9, Okamoto teaches substantially the entire claimed structure of claims 1 and 2 above except explicitly stating that the chip comprises a transponder.

Loeffler teaches that a transponder can be integrated as an IC device (transponder IC, col. 3, lines 16-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transponder device taught by Loeffler in the structure of Okamoto in order to form a transponder device.

Regarding claim 10, Okamoto teaches substantially the entire claimed structure of claims 1 and 2 above including the conductive layer comprises an aerial.

The combined structure Okamoto and Loeffler teaches a transponder that is integrated as an IC device. Since a transponder in general is equipped with an antenna structure, the combined structure Okamoto and Loeffler would inherently have an aerial that is made of a conductive material.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto, in view of Loeffler et al. US patent No. 5,838,074.

Regarding claim 11, Okamoto teaches substantially the entire claimed structure of claims 1, and 9-10 above except explicitly stating that a chip having a transponder attached to the baseplate.

Since the combined structure of Okamoto and Loeffler teaches that a transponder can be integrated as an IC device, t would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transponder device taught by Loeffler in the structure of Okamoto in order to form a transponder device.

10. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto, Nakaoka and in view of Loeffler.

Okamoto teaches substantially the entire claimed structure of claims 1, 3, 7-8 and 9-10 above including the height of the chip is so low that it is rendered flexible.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D and E are cited as being related to semiconductor packaging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
November 28, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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